IN THE CLAIMS

1. (Previously Amended) An integrated circuit comprising:

a plurality of pixel circuits arranged in rows and columns;

a plurality of first lines, each first line connected to a corresponding column of pixel circuits; and

a plurality of second lines, each second line connected to a corresponding row of pixel circuits,

wherein the plurality of first lines are formed such that each first line extends over the plurality of second lines at corresponding crossover locations, and

wherein an air-gap is defined at each crossover location that separates each first line from the plurality of second lines, wherein each air-gap extends from a top surface of a corresponding second line to a bottom surface of said each first line.

2. (Previously Amended) The integrated circuit according to Claim 1, wherein each pixel circuit includes an access transistor and a pixel element, wherein the access transistor includes a gate terminal connected to an associated first line, a first terminal connected to the pixel element, and a second terminal connected to an associated second line.

3. (Original) The integrated circuit according to Claim 2, wherein the access transistor comprises one of amorphous silicon and polysilicon.

4. (Original) The integrated circuit according to Claim 2, wherein the access transistor of each pixel circuit comprises a self-aligned thin-film transistor.

5. (Original) The integrated circuit according to Claim 2, wherein each of the plurality of pixel circuits also

comprises a charge sensing region that is separated from the associated second line by a buried insulator layer comprising a resin derived from B-staged bisbenzocyclobutene monomers.

6. (Original) The integrated circuit according to Claim 2, wherein the integrated circuit comprises a medical image sensor array.

7. (Original) The integrated circuit according to Claim 2, wherein each pixel element comprises an amorphous silicon sensor, and each pixel circuit further comprises a phosphor converter located over the amorphous silicon sensor.

8. (Previously Amended) An image sensor array comprising:

a plurality of pixel circuits arranged in rows and columns, each pixel circuit including an access transistor;

a plurality of gate lines, each gate line connected to the access transistors of a corresponding column of pixel circuits; and

a plurality of data lines, each data line connected to the access transistors of a corresponding row of pixel circuits,

wherein the plurality of data lines are formed such that each data line overlaps the plurality of gate lines at corresponding crossover locations, and

wherein an air-gap is defined at each crossover location that separates each data line from the plurality of gate lines such that each air-gap extends from a top surface of a corresponding gate line to a bottom surface of said each data line.

9. (Original) The image sensor array according to Claim 8,

wherein the plurality of gate lines are formed from a first metal layer, the plurality of data lines are formed from a second metal layer such that the data lines are located above the first metal layer, wherein each of the plurality of pixel circuits also comprises a sensor including an amorphous silicon (a-Si:H) layer formed on a metal plate, and

wherein the metal plate is formed from a third metal layer formed after the first and second metal layers.

10.(Original) The image sensor array according to Claim 8, further comprising a strengthening insulator formed on the plurality of data lines at the crossover locations.

21. (Previously Added) The image sensor array according to Claim 8, wherein the access transistor of each pixel circuit comprises a self-aligned thin-film transistor.

22. (Previously Added) The image sensor array according to Claim 21, wherein the self-aligned thin-film transistor of each pixel circuit comprises:

an amorphous silicon (a-Si:H) layer including a relatively undoped first region located over an associated gate line, the first region being located between a doped second region and a doped third region; and

an optical filter island located over the first region, the optical filter island comprising at least three layers having at least two indexes of refraction and being arranged such that the optical filter island is reflective of a first radiation wavelength and transmissive of a second radiation wavelength.

23. (Previously Added) The image sensor array according to Claim 22,

wherein each of the plurality of pixel circuits also comprises a sensor including an amorphous silicon (a-Si:H) layer formed on a metal plate,

wherein the metal plate is connected to the doped second region of the self-aligned thin-film transistor, and

wherein an associated data line is connected to the doped third region of the self-aligned thin-film transistor.

24. (Previously Added) The image sensor array according to Claim 8, wherein each of the plurality of pixel circuits also comprises a charge sensing region that is separated from the associated data line by a buried insulator layer comprising a resin derived from B-staged bisbenzocyclobutene monomers.

25. (Previously Added) The image sensor array according to Claim 24, wherein the buried insulator layer has a thickness of 3 to 5 microns.

26. (Previously Added) The image sensor array according to Claim 24, wherein the charge sensing region of each of the plurality of pixel circuits comprises an amorphous silicon (a-Si:H) layer.

27. (Currently Amended) The image sensor array according to Claim 8,

wherein the image sensor array further comprises spaced-apart data line support pads [formed from the first metal layer], and

wherein each spaced-apart data line support pad contacts an associated data line.

28. (Previously Added) An image sensor array comprising:

a substrate having an upper surface defining a plane;

a plurality of pixel circuits arranged in rows and columns over the upper surface of the substrate;

a plurality of first lines, each first line being formed on the upper surface of the substrate and connected to a corresponding first group of said pixel circuits; and

a plurality of second lines connected to a corresponding second group of said pixel circuits, each second line including:

first portions supported by the upper surface of the substrate, and

second portions extending over the plurality of first lines at corresponding crossover locations such that an air gap is defined at each said crossover location between a top surface of a corresponding first line and a bottom surface of the corresponding second portion of said each second line.

29. (Previously Added) The image sensor array according to Claim 28, further comprising a plurality of support pads, each support pad being formed on the upper surface of the substrate and contacting a corresponding first portion of an associated second line.

30. (Previously Added) An image sensor array comprising:

a substrate having an upper surface defining a plane;

a plurality of pixel circuits arranged in rows and columns over the upper surface of the substrate;

a plurality of first lines, each first line being formed over the upper surface of the substrate and connected to a corresponding first group of said pixel circuits;

a plurality of support pads, each support pad being formed over the upper surface of the substrate; and

a plurality of second lines connected to a corresponding second group of said pixel circuits, each second line including:

a plurality of first portions, each first portion contacting a corresponding support pad, and

second portions extending between adjacent first portions such that each second portion is freely supported by an associated pair of adjacent first portions, wherein each second portion extends over a corresponding first line such that an air gap is defined between the corresponding first line and said each second portion.